

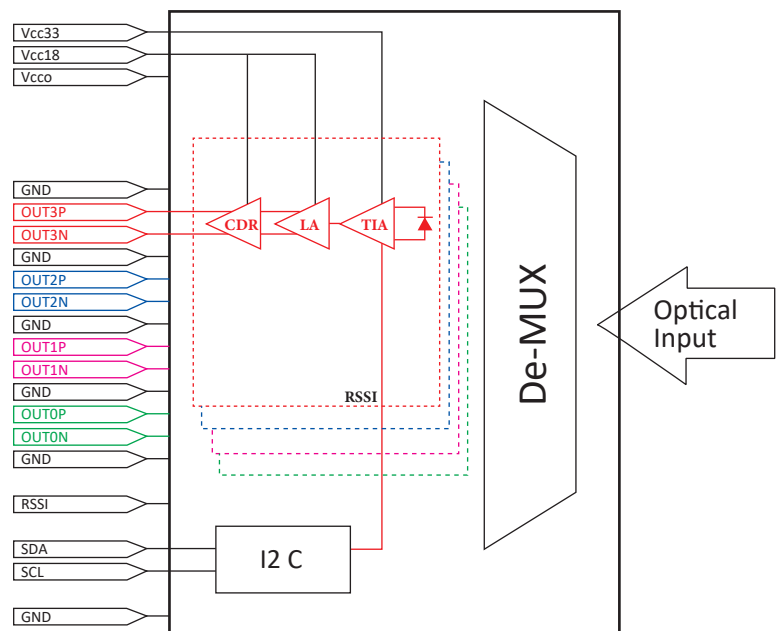
Key Features

- Up to 25.78125 ±100 ppm Operation (NRZ)
- PIN Photodiode (PIN-PD) Base Quad ROSA for CWDM4
- Integrated TIA/LA/CDR
- Programmable Output Swing, Squelch and De-Emphasis
- 2 Wire Communication (Up to 400 kHz)
- CWDM4 Optical De-MUX Integrated
- Pigtail with LC Connector
- SMT Style for Electrical RF Signals

Applications

- CWDM4 MSA
- QSFP28/CFP2/CFP4 Transceiver Modules
- On Board Optics

Modular Block Diagram



Optical and Electrical Characteristics

T_c = 0°C to 80°C, (unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.
Bit Rate		NRZ, each lane		25.781 Gb/s	
Operational Case Temperature	T _c		0°C	25°C	80°C

PD

Peak Wavelength for L0	L ₀ ¹	for L0	1264.5 nm	1271 nm	1277.5 nm
	L ₁ ¹	for L1	1284.5 nm	1291 nm	1297.5 nm
	L ₂ ¹	for L2	1304.5 nm	1311 nm	1317.5 nm
	L ₃ ¹	for L3	1324.5 nm	1331 nm	1337.5 nm
PD Responsivity	R	CW	TBD	TBD	TBD
Damage threshold, each lane ²	P _d	CW	3.5 dBm		
Maximum Overload, each lane ¹	P _{max}	OMA	2.5 dBm		
Minimum Sensitivity, each lane ^{1, 3}	P _{min}	OMA		-11.3 dBm	
SRS eye mask definition (X1, X2, X3, Y1, Y2, Y3) ^{1, 4, 5}		4 th Bessel		Refer to Figure1 (0.39, 0.5, 0.5, 0.39, 0.39, 0.4)	
Optical Return Loss	ORL	λ = 1300 nm			26 dB

TIA/LA/CDR

Core Power Supply Voltage (1.8 V)	V _{cc18,Vcco}		1.71 V	1.80 V	1.89 V
TIA Power Supply Voltage (3.3 V)	V _{cc33}		2.97 V	3.3 V	3.47 V
Differential Output Impedance Termination	R _{TERM}			100 ohm	
Differential Output Amplitude ⁸	R _x x	AC	300 mVppd	800 mVppd	930 mVppd
Rx x Rise/Fall Time ¹²	T _{RISE} /T _{FALL}	20~80%		16 psec	20 psec
Output Differential Return Loss ⁶	S ₂₂				TBD
RSSI Range	RSSI _{Range}		4 μA		504 μA
Program Output De-emphasis ^{8, 12}	DE		0 dB		7.5 dB
Total Output Jitter ¹⁰	t _{JIT}				TBD
Loss Of Signal ^{7, 8}	LOS				TBD
LOS Hysteresis ^{7, 8}	LOS _{HYST}		1.5 dB		2.5 dB
LOS Assert Time ⁹	T _{ast}				100 μsec
LOS De-assert Time ⁹	T _{deast}				100 μsec
CDR Lock Time	T _{LOCK}			0.7 msec	2 msec
LOL Timing from occurrence to triggering ¹¹	T _{LOCK}				0.5 msec

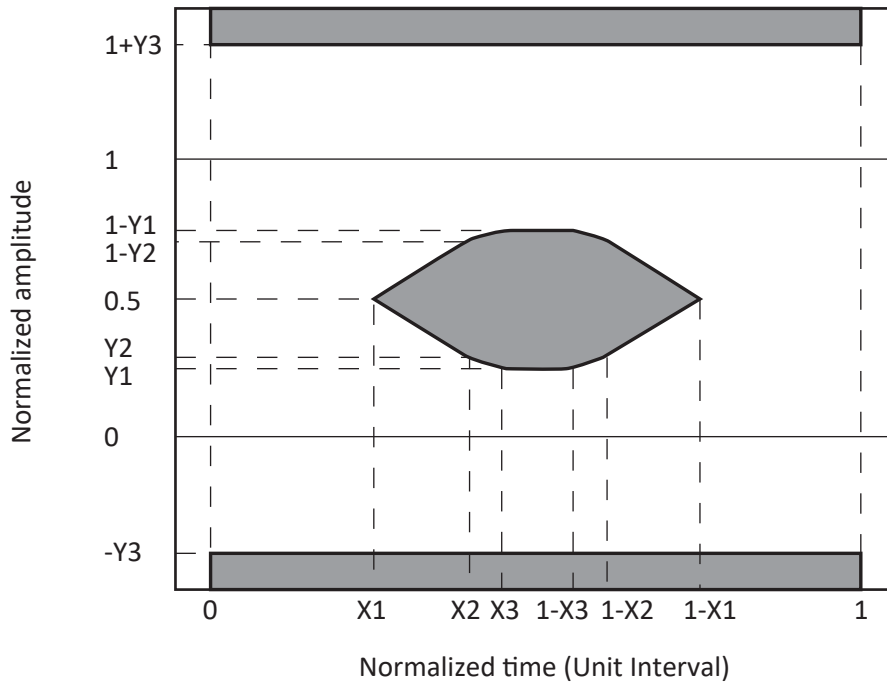
Optical and Electrical Characteristics

T_c = 0°C to 80°C, (unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.
I2C					
CMOS Output Logic High	V _{OH_CMO5}	I _{OH} = 4 mA	1.5 V	1.7 V	1.92 V
CMOS Output Logic Low	V _{OL_CMO5}	I _{OH} = 4 mA		0 V	0.3 V
Open Drain Output Logic High	V _{OH_OD}	I _{OH} = 4 mA	0.8xV _{CC-EXT}		V _{CC-EXT}
Open Drain Output Logic Low	V _{OL_OD}	I _{OH} = 4 mA		0 V	0.3 V
Input Logic High	V _{IH}		0.75xV _{CC18}		3.465 V
Input Logic Low	V _{IL}		0 V		0.2xV _{CC18}
Total Power Dissipation	P _{total}			0.71 W	TBD

- 1: 25.8Gbps, PRBS=2³¹-1.
- 2: The receiver shall be able to tolerate, without damage, continuous exposure to an optical signal having this average power level.
- 3: BER=5E-5 and normative specification.
- 4: BER=5E-5, Vertical eye closure penalty = 1.9 dB, J2 Jitter = 0.33 UI and J4 Jitter = 0.48 UI.
- 5: See mark in Figure1.
- 6: Measured using MACOM EVM and an output latched high or low.
- 7: The LOS assert/de-assert levels are independent of CDR enable or CDR bypass modes.
- 8: Typical programmable range.
- 9: Minimum of 6 dB change in optical signal.
- 10: CDR enabled.
- 11: The time it takes to assert the LOL from valid input data to invalid input data. The valid input data is data within range covered by the data rates.
- 12: Measured with 100 Ω differential load.

Figure 1. SRS Eye Mask

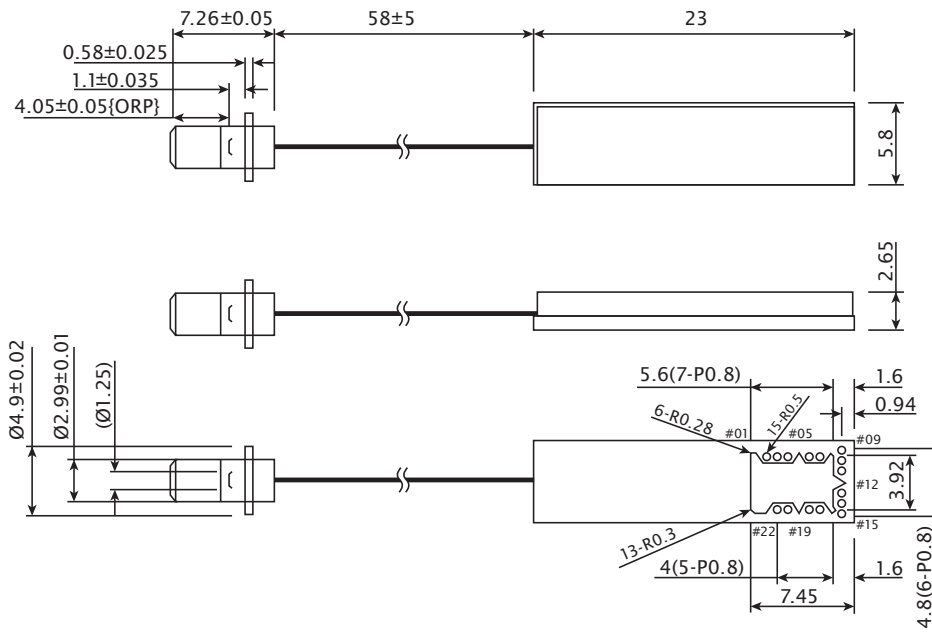


Absolute Maximum Ratings

T_c = 25°C, (unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.
Maximum Optical Input Power	PIN	Each lane, CW	4 dBm	
Core Power Supply Voltage (1.8V)	Vcc18, Vcco		-0.5 V	2 V
TIA Power Supply Voltage (3.3V)	Vcc33		-0.5 V	4 V
DC Input Voltage (CMOS)	VIN CMOS	SCL	GND-0.5 V	3.8 V
Maximum Current from RSSI	IRSSI		4 mA	
Maximum Current from OUTP/N	Iout		20 mA	
Storage Temperature	Tstg		-40 degC	85 degC
Electrical Discharge Voltage(HBM)	VESD, HBM			TBD

Dimensions



Unit: mm

Pin Configuration

Pin#	Symbol	Description	Pin#	Symbol	Description
1,5,8,9,12,15,16,19,22	GND	Ground	11	OUT2N	negative data output for L1
2	Vcc33	+3.3 V power supply	13	OUT1P	positive data output for L2
3	NC	No Connect	14	OUT1N	negative data output for L2
4	Vcco	+1.8 V power supply	17	OUTOP	positive data output for L3
6	OUT3P	positive data output for L0	18	OUTON	negative data output for L3
7	OUT3N	negative data output for L0	20	SCL	two-wire serial interface clock
10	OUT2P	positive data output for L1	21	SDA	two-wire serial interface data

OptiWorks Headquarters

OptiWorks, Inc.

47211 Bayside Parkway, Fremont, CA 94538, USA
Phone +1 510 438 4560
sales@optiworks.com
www.optiworks.com

OptiWorks (Kunshan) Co., Ltd.

No. 168, Nanhe Rd., Kunshan Economic & Technology Development Zone, Kunshan City, Jiangsu 215300, China
Phone +86 512 5763 0863
contact@optiworks.com

© 2020 BizLink Group. All rights reserved.
BizLink, OptiWorks, and other trademarks are the trademarks of BizLink Group or its subsidiaries.
Performance is based on target specifications, simulated results, and/or prototype measurements. Commitment to develop is not guaranteed.
Specifications are subject to change without prior notice. April 2020

OptiWorks (Shanghai) Co., Ltd.

Room 810-811, Changchun Business Building, No. 953 Qinzhou North Road, Shanghai 200233, China
Phone +86 021 6485 8787
contact@optiworks.com